Electronic Version
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Claims

[c1] What is claimed is:

1. A multi-stage delay clock generator comprising:

a plurality of delay cells, each delay cell generating a delay signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal where a first delay cell among the plurality of delay cells receives an external clock signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell;

a phase detector, responsive to the external clock signal and a feedback clock signal, for generating a lock control signal;

an integrator, responsive to the lock control signal, for generating the delay control signal; and

a control unit for programming the delay cells.

[c2] 2. The multi-stage delay clock generator in claim 1, wherein the integrator comprises:

a delay counter, responsive to the lock control signal, for generating the delay control signal;

a plurality of multiplexers, responsive to the delay control signal, for outputting a select signal; and

a plurality of latches, responsive to the select signal, for outputting a lock signal to the plurality of delay cells and to a subsequent multiplexer.

[c3] 3. The multi-stage delay clock generator in claim 1, wherein a range of the first delay cell is greater than a range of a maximum delay target from the external clock signal.

[c4] 4. The multi-stage delay clock generator in claim 1, wherein the delay step of a last delay cell is smaller than a system jitter.

[c5] 5. The multi-stage delay clock generator in claim 1, wherein a delay step of the first delay cell is determined by a total number of programming bits.

[c6] 6. The multi-stage delay clock generator in claim 5, wherein the total number of programming bits is a value from dividing the range of the maximum delay target by the delay step of the first delay cell.

[c7] 7. The multi-stage delay clock generator in claim 1, wherein a number of delay cells is dependent on a resolution of the last delay cell.

[c8] 8. The multi-stage delay clock generator in claim 1 further comprises a delay offset electrically coupled to a

last delay cell for generating an offset delay signal.

[c9] 9. A method for generating a delay signal comprising:
comparing an external clock signal and a feedback to determine a maximum delay target;
dividing a first delay cell into a plurality of delay steps according to a number of programming bits that is obtained from the maximum delay target;
repeatedly dividing a subsequent delay cell into a plurality of smaller delay steps according to a size of the delay steps of the first delay cell, wherein each subsequent delay cell comprises smaller and smaller delay steps;
comparing the external clock signal to the delay step of the delay cells by a tunable detecting window to output a lock control signal;
latching the delay cell according to the lock control signal;
adjusting a width of the tunable detecting window for the subsequent delay cells; and
sending a delay control signal to the delay cells.

[c10] 10. The method of claim 9 further comprises initially programming the delay cells.

[c11] 11. The method of claim 10, wherein initially programming the delay cells comprises:
asserting a reset signal to the first delay cell;

calibrating the first delay cell;
latching a delay value of the first delay cell; and
asserting the reset signal to the subsequent delay cell until all delay cells are calibrated.

[c12] 12. The method of claim 9, wherein a delay step of the first delay cell is determined by a total number of programming bits.

[c13] 13. The method of claim 9 further comprises a delay offset electrically coupled to a last delay cell for generating an offset delay signal used for preventing a trap causing lock-failure.

[c14] 14. A multi-stage delay clock generator for generating a delay signal, comprising:
a first delay chain for generating a first delay signal, in response to an external clock signal and a first delay control signal, comprising a plurality of delay cells, each delay cell generating a delayed clock signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell;
a second delay line for generating a second delay signal, in response to a second delay control signal and a feedback clock signal, comprising a plurality of delay cells,

each delay cell generating a delayed clock signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell;
a first phase detector, responsive to a delayed external clock signal and the first delay signal, for generating a first control signal;
a second phase detector, responsive to a delayed feedback clock signal and the second delay signal, for generating a second control signal;
an integrator, responsive to the first and the second control signal, for generating the first delay control signal and the second delay control signal; and
a control unit for programming the delay cells.

[c15] 15. The multi-stage delay clock generator in claim 14, wherein the integrator comprises:
a delay counter, responsive to the lock control signal, for generating the delay control signal;
a plurality of multiplexers, responsive to the delay control signal, for outputting a select signal; and
a plurality of latches, responsive to the select signal, for outputting a lock signal to the plurality of delay cells and to a subsequent multiplexer.